WHAT IS CLAIMED IS:

1. An insulated gate field effect transistor having a gate electrode in a channel area between a first and second types of source areas thereof, wherein:

said channel area comprises an area portion free from lapping over the gate electrode in plan.

2. The field effect transistor according to claim 1, wherein:

said channel area is made of a polycrystal silicon film.

3. The field effect transistor according to claim 2, wherein:

the area portion of said channel area free from lapping over the gate electrode in plan has a length longer than a crystal grain size of the polycrystal silicon that composes said channel area.

4. The field effect transistor according to claim 1, wherein:

said channel area is made of an intrinsic semiconductor.

5. The field effect transistor according to claim 4, wherein:

the area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

6. The field effect transistor according to claim 1, wherein:

said gate electrode is provided on an

opposite side of a substrate, which holds said channel area, from said channel area.

7. The field effect transistor according to claim 1, wherein:

said gate electrode is provided between said channel area and said substrate that holds said channel area.

8. The field effect transistor according to claim 1, wherein:

at least a part of said gate electrode laps over one of said first and second source areas in plan.

9. An insulated gate type field effect transistor having a gate electrode in a channel area between a first and a second types of source areas thereof, wherein:

said gate electrode comprises two separate subgate electrodes disposed on the respective sides of said first and second types of source areas in a direction in which said channel area extends.

10. The field effect transistor according to claim 9, wherein:

said channel area is made of an intrinsic semiconductor.

11. The field effect transistor according to claim 10, wherein:

the area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

12. A double field effect transistor device of an

insulated gate type, comprising:

a channel area taking a virtually H-type form in plan;

a first pair of source areas different in conductive type respectively formed at opposite ends of one of a pair of parallel strips that composes a part of the H;

a second pair of source areas different in conductive type respectively formed at opposite ends of the other of said pair of parallel strips that composes a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductive type; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that composes a part of the H and a central link of the H that combines said pair of parallel strips.

13. The field effect transistor according to claim 12, wherein:

said channel area is made of an intrinsic semiconductor.

14. The field effect transistor according to claim 13, wherein:

the area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

15. An image display apparatus comprising a

display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein.

at least part of said controller is of an insulated gate type having a gate electrode in a channel area between a first and second types of source areas thereof; and

said channel area comprises an area portion free from lapping over the gate electrode in plan.

16. An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein.

at least part of said controller is of an insulated gate type having a gate electrode in a channel area between a first and second source areas thereof; and

said channel area comprises an area portion free from lapping over the gate electrode in plan; and said apparatus comprising:

an image control unit of said display unit being of an insulated gate type, said image control unit comprising:

a channel area taking a virtually H-type

form;

a first pair of source areas different in conductive type respectively formed at opposite ends of one of a pair of parallel strips that composes a part of the H;

a second pair of source areas different in conductive type respectively formed at opposite ends of the other of said pair of parallel strips that composes a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in conductive type; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that composes a part of the H and a central link of the H that combines said pair of parallel strips.